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REMARKS

Applicants concurrently file herewith a Petition (and fee) for a three-month extension of time and a Notice of Appeal (and fee).

Applicants gratefully acknowledge Examiner Vy and Supervisory Patent Examiner Ip for taking time from their busy schedule on February 20, 2004, for a telephone interview with Applicants' representative.

During that telephone interview, Applicants' representative explained that the wording "... to make said voltage difference small", that is the basis for the rejection under 35 USC §112, second paragraph, is merely wording chosen by the inventor to describe the concept inherent in a negative feedback loop. Applicants' representative also submitted that one of ordinary skill in the art would readily understand the concept that Applicants were describing and that, therefore, the "metes and bounds" of the invention described in the claims were readily understandable.

With this explanation, Examiners Ip and Vy are understood as having agreed that one of ordinary skill in the art would understand the wording of the claims, and that the rejection based on 35 USC 112, second paragraph, would be formally withdrawn via a facsimile correspondence with Applicants' representative.

Second, Applicants' representative also raised the issue that the rejection under 35 USC §112, second paragraph, was a newly-raised issue that was not warranted by the changes to the claims in the previous amendment and that, therefore, it would be improper to make the rejection final. It was agreed that the withdrawal of the rejection renders this issue moot and that the status of the rejection, therefore, remains final.

As a third discussion focus during this telephone interview, the Examiners focused the prior art rejection onto the prior art shown in Figure 8 of the present Application. As best understood, it is the position of the Examiners that the switch SW0 shown in Figure 8 causes a dual time constant for the amplifier circuit shown in Write Block 10. As best understood, based on the Examiners' comments during this telephone interview, the Examiners consider that a sudden change in the input signal due to, for example, switching would cause the amplifier to have a second time constant.

Applicants' representative submitted that, to one of ordinary skill in the art, the time constant of an amplifier is determined, not by the input signal, but by the composition of the

feedback loop of the amplifer, shown in Figure 8 as fixed components C and R2.

Although the Examiners disagreed with this position during the telephone interview, this technical issue seems to be the major issue of the prior art rejection, and is discussed more in the comments below. Regardless of this difference of opinion in this technical issue, Applicants again wish to acknowledge the Examiners for taking the time to discuss the pressing issues that are significant in the present Application, particularly in view of the very short time remaining before the present Application automatically abandons, in accordance with the shortened statutory requirements.

Entry of this Amendment is proper under 37 CFR §1.116, since no new claims or issues are presented, since the claim amendments above are merely clerical in nature, and this Amendment places on record the Applicants' position in what seems the remaining issue dealing with the prior art rejection.

That is, it is necessary that this Amendment be entered in the record for purpose of allowing the Examiner to respond and, thereby, clarify the issues for appeal.

Claims 1-22 are all of the claims presently pending.

As best understood, in accordance with the telephone interview dated February 20, 2004, and presuming the withdrawal of the rejection under 35 USC §112, second paragraph, claims 8-14 and 16-18 are allowed, as based on the Examiner's statements in Paragraph 5 on page 6 of the Office Action dated August 27, 2004.

Applicants gratefully acknowledge the Examiner's indication that claims 3-7 would be allowable if rewritten in independent form. Applicants reserve the right to rewrite these claims at a later date to overcome this rejection and to place claims 3-7 into condition for allowance.

As best understood, claims 1- 2, 15, and 19-20 currently stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kamioka et al. (U.S. Patent No. 5,831,951) and by the Applicants' Admitted Prior Art (APA).

Claims 21 and 22 are stated as being rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 4,950,268 to Rink et al. However, the rejection actually additionally addresses claims 1-3 and 8-10 and fails to address claim 21. Therefore, Applicants request that, should this rejection based on Rink be maintained, that the Examiner clarify the claims being rejected for purpose of appeal.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

Applicants' invention, as defined for example in a non-limiting embodiment of independent claim 1 (and substantially similarly by independent claim 15) is directed to a power control circuit for a laser diode, including an amplifier circuit producing at an output terminal thereof an output voltage responsive to a voltage difference between a reference voltage and a feedback voltage that is indicative of an optical power generated by the laser diode in response to a driving current flowing therethrough.

A driving circuit responds to the output voltage to control the driving current so as to make the voltage difference small. The amplifier circuit drives the output terminal with a first time constant during a steady operation and with a second time constant that is smaller than the first time constant upon initiation and before the steady operation.

With such features, an operation mode can be quickly shifted and stabilization in the optical output of a laser diode can be improved (e.g., see page 8, lines 1-14 and 25-28; page 9, lines 1-9 and 21-27; page 10, lines 1-8; page 12, lines 1-27; and page 13, lines 1-3 of the present application).

The conventional systems, such as those discussed below and in the Related Art section of the present application, do not have such a structure, and fail to provide for such an operation.

Such features are not taught or suggested by any of the cited references.

II. THE 35 USC §112, SECOND PARAGRAPH, REJECTION

In the Office Action dated August 27, 2003, all claims stand rejected under 35 USC §112, second paragraph, for being indefinite. In accordance with the telephone interview dated February 20, 2004, with Supervisory Patent Examiner Ip and Examiner Vy, this rejection has been withdrawn. Therefore, Applicants make no claim amendments to address this rejection.

III. THE PRIOR ART REJECTIONS

The Rejection Based on Kamioka

The Examiner alleges that Kamioka anticipates claims 1, 2, 15, 19, and 20 and points specifically to Figure 5 in Kamioka. However, although this figure illustrates an integrator circuit allegedly having two time constants, it clearly fails to be incorporated into the

application that is described in these claims. Although the Examiner is allowed to provide a reasonably broad interpretation of claim language, this interpretation and the interpretation of the prior art reference must be consistent with that of one of ordinary skill in the art.

That is, as described at lines 53-58 of column 4 of Kamioka, Figure 5 illustrates integrator 24 that is shown in Figure 4. According to lines 40-41 of column 4, Figure 4 illustrates binarization block 11, which is, in turn, shown in Figures 1 and 2.

As can clearly be seen in Figure 1, binarization block 11 is not at all related to the laser diode used for reading and writing data to/from the optical disk 1. As clearly described at lines 8 and 9 of column 4, the servo loop that includes servo control 7 is used to control the focusing and location of the optical pickup 3 on actuator 8.

This circuit is entirely different from a feedback loop for controlling the current of the laser diode. Therefore, nothing in Figures 1-15 of Kamioka demonstrates the environment described by the independent claims of the present Application, in which the current of the laser diode is being controlled in a two-switch feedback loop.

Applicants submit that, as would be interpreted by one of ordinary skill in the art, the Examiner stretches the point by characterizing Kamioka as addressing a "... control circuit for a laser diode". Although there may be a laser diode associated with the apparatus shown in Figure 1, the control of the current of that laser diode is not the purpose of Kamioka.

The present invention of claim 1 (e.g., see preamble and body of claim) clearly defines a control circuit for the power of the laser diode. Again, Kamioka controls only focusing and location of an optical pickup. The Examiner is not entitled to ignore the plain meaning of the claim language.

Hence, turning to the clear language of the claims, in Kamioka there is no teaching or suggestion of:

> "*A power control circuit for a laser diode, comprising: an amplifier circuit producing at an output terminal thereof an output voltage responsive to a voltage difference between a reference voltage and a feedback voltage that is indicative of an optical power generated by said laser diode in response to a driving current flowing therethrough; and a driving circuit responding to said output voltage to control said driving current so as to make said voltage difference small, said amplifier circuit driving said output terminal with a first time constant during a steady operation and with a second time constant that is smaller than said first time constant upon initiation and before said steady operation*",

as required by claim 1. Independent claim 15 contains similar language.

For the reasons stated above, independent claim 1 (and substantially similarly independent claim 15) of the claimed invention are fully patentable over Kamioka.

Further, dependent claims 2 and 19-20 when taken in combination with independent claim 1 (and similarly new claims 21-22) define additional novel limitations.

The Rejection Based on APA

Relative to the rejection based on the APA shown in Figures 7 and 8 of the present Application, the current control loop for laser diode 1 clearly contains no switches or other mechanism for two time constants in this control loop when, for example, amplifier module 10 is controlling the laser diode 1.

That is, as explained during the telephone interview on February 20, 2004, with Supervisory Patent Examiner Ip and Examiner Vy, it is the Applicants' position that one of ordinary skill in the art would readily understand that independent claim 1 specifically states that the amplifier circuit itself has two different time constants.

As best understood from the Examiners' remarks during this telephone interview and upon further reflection, Applicants submit that, perhaps, the following discussion might clear up some basic confusion that would seem to have been exposed in the interview:

First, it is noted that, as best understood during the telephone interview, the Examiners consider that there is a different time constant during, for example, the write mode versus the read mode.

In response, Applicants submit that this is indeed a correct statement. That is, Applicants fully concur with the Examiners' position that a different amplifier module 10, 20, 30 controls the laser diode 1 during different modes, as clearly shown in Figure 8 and further explained at lines 19-23 of page 6.

However, Applicants submit that this is not what is being claimed.

What Applicants consider as being a significant contribution to the art provided by the present invention, is the additional capability of having two time constants for the amplifier itself, such as in the mode module 10, 20, 30 shown in Figure 8 (e.g. write mode, erase mode, read mode). Each time constant is controlled based upon whether that mode amplifer is currently involved in a steady state or a transient state.

This is an entirely different concept than stating that the laser diode 1 responds to a different time constant during the different modes, such as read, write, and erase.

The switch SW0 shown in write block 10 of Figure 8 does not provide a second time constant. Rather, as explained at line 23 of page 4 through line 6 of page 5, the effect of this switch SW0 is that of merely providing the write current reference as the input V2 into the amplifer during the write mode. In any other mode, switch SW0 grounds out the V2 input so that the amplifier 4 output is not a significant input to the laser diode 1.

Thus, there is no second time constant caused by switch SW0 in Figure 8. The lack of a second time constant is clearly shown in Figure 9, wherein is shown, in the right side WRITE cycle, the single time constant effective during the write mode.

In contrast, Figure 2 shows an exemplary set of voltage response curves resulting from the exemplary embodiment shown in Figure 1. In comparing Figure 2 with Figure 9, it should be readily apparent that the right side WRITE cycle has two time constants, one for the initiation portion and one for the steady operation portion.

It is also pointed out that the improvement in the rise time is clearly shown in comparing the value of 3 μsec for the rise time in Figure 2, versus the "tens of μsec, or more" that is shown in Figure 9.

To one of ordinary skill in the art, this rise time difference is clearly due to the switching of switch SW0 shown in Figure 1 and is a significant improvement in rise time over the prior art shown in Figure 8.

Given the above clarification, Applicants request that the Examiner place specific details on the record, for purpose of Appeal, should the Examiner wish to maintain this rejection based on APA.

Hence, turning to the clear language of the claims, in APA there is no teaching or suggestion of:"... said amplifier circuit driving said output terminal with a first time constant during a steady operation and with a second time constant that is smaller than said first time constant upon initiation and before said steady operation", as required by the independent claims 1 and 15.

For this reason, independent claim 1 (and substantially similarly independent claim 15) of the claimed invention are fully patentable over APA, and, dependent claims 2 and 19-20, when taken in combination with independent claim 1, (and similarly claims 21-22) define additional novel limitations.

The Rejection Based on Rink

Relative to the rejection based on Rink and as best understood, the Examiner alleges that Figures 2 and 3 of Rink anticipate the present invention as defined by various claims. However, similar to the comments above for Kamioka, the Examiner's evaluation must be consistent with the plain meaning of the language of the claims and prior art references, as interpreted by one of ordinary skill in the art.

Applicants submit that, upon closer scrutiny, one of ordinary skill in the art would be quite confused as to how the Examiner is attempting to apply these two figures so that any of the claims in the present Application read upon them.

First, it is noted that Figure 2 is described at lines 3-7 of column 3 as demonstrating a "... *temperature safety circuit that senses an overtemperature condition in the laser system and shuts off power to the laser power supply*". According to the description beginning at lines 64 of column 5, this Figure 2 is not related to a control circuit for power of a laser diode, except that, upon sensing an overtemperature, using infrared photodetector 57, this circuit pulls down AND input 32R, which, in turn chops "... *the duration of the next successive laser pulse in response to the previous temperature level*".

Relative to the Examiner's description that C_2 causes the amplifier 64 to operate with two separate time constants, Applicants submit that, as clearly described at lines 46-48 of column 6, the purpose of the two switches controlled by C_2 is not to provide two time constants but to reset the integrator formed by capacitor 66 with op amp 64 so as "... *to reset the integration product to zero prior to each laser pulse*."

Therefore, to one of ordinary skill in the art, the circuit shown in Figure 2 does not have two operational time constants, since the reset period between laser pulses would not be a "time constant", as that term is understood by one of ordinary skill in the art. If anything, one of ordinary skill in the art would consider the shorting out of the capacitor as being a transient during which time the laser diode is not operating and would also consider that the integrator circuit 64,66 is also not operating.

Hence, turning to the clear language of the independent claims, there is no teaching or suggestion in Rink of: "...said amplifier circuit driving said output terminal with a first time constant during a steady operation and with a second time constant that is smaller than said first time constant upon initiation and before said steady operation", as required by claims 1 and 15. Independent claim 21 has similar language concerning two separate time constants.

Relative to the rejection for claim 22, in which the Examiner relies upon Figure 3 of Rink, it is noted that this figure does not illustrate the amplifier circuit of Figure 2, so that a rejection of a claim depending from claim 21 is inherently improper.

It is also noted that, to one of ordinary skill in the art, Figure 3 of Rink fails to show a "... a first resistor coupled to an input end of said operational amplifier; and a second switch coupled to said input end of said operational amplifier through said first resistor ", as required by the plain meaning of the claim language.

Therefore, Applicants submit that one of ordinary skill in the art would not consider that either Figure 2 or Figure 3 of Rink teaches or suggests the present invention, as defined by the independent claims.

For the reasons stated above, the claimed invention is fully patent able over the cited references.

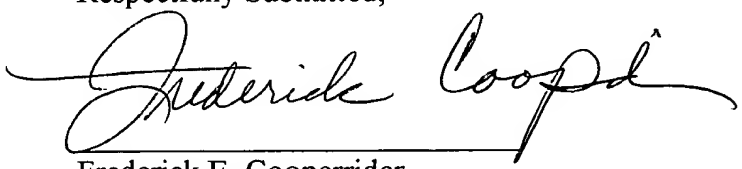
IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicants submit that claims 1-22, all the claims presently pending in the application, are parentally distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,



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